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Modeling of spiking analog neural circuits using organic semiconductor thin film transistors with silicon oxide nitride semiconductor gates

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ABSTRACT

This paper uses the results of the characterization of amorphous semiconductor thin film transistors (TFTs) with the quasi-permanent memory structure referred to as silicon oxide nitride semiconductor (SONOS) gates, to model spiking neural circuits. SONOS gates were fabricated and characterized. In addition, MOSFETs using organic copper phthalocyanine (CuPc) were fabricated with these SONOS gates to demonstrate proof of concept performance. Analog spiking circuits were then modeled using these low performance TFTs to demonstrate the general suitability of organic TFTs in neural circuits. The basic circuit utilizes a standard comparator with charge and discharge circuits. A simple Hebbian learning circuit was added to charge and discharge the SONOS device. The use of these elements allows for the design and fabrication of high-density 3-dimensional circuits that can achieve the interconnect density of biological neural systems.

1. Introduction

The main purpose of this work is to; first, verify that amorphous organic transistors can be produced with silicon oxide nitride oxide semiconductor (SONOS) gates, and, second, to demonstrate that these transistors can be used to produce spiking analog neural circuits with imbedded Hebbian learning. This work includes the fabrication and characterization of parallel plate capacitors with the quasi-permanent memory structure (SONOS) gates and organic TFTs using copper phthalocyanine (CuPc) with these SONOS gates. These initial results were then used to model spiking neural circuits with a Hebbian learning ability. MOSFETs using these materials have been characterized and have been shown to have appropriate voltage-current characteristics [1–4]. Through the appropriate selection of contact metals, p and n type transistors can be produced and allow for the manufacture of CMOS circuits. The use of amorphous materials allows for the fabrication of stacked, 3-dimensional circuits which can greatly increase the circuit density allowing for circuits that can achieve the interconnect density of biological neural systems. A simple Hebbian learning circuit can be added to charge and discharge the SONOS device. This comprises a short pulsing circuit that induces tunneling into the SiN charge storage layer. This then acts to shift the threshold voltage of the transistor and effectively increase (or decrease) the synaptic weight. In this work we confirmed the functionality of SONOS structures using CuPc semiconductor materials and demonstrate the usefulness in modeled analog spiking neural circuits.

2. Background

The SONOS structure has been characterized as a quasi-static memory device [5–9]. The structure allows for electron or hole tunneling through a thin oxide from

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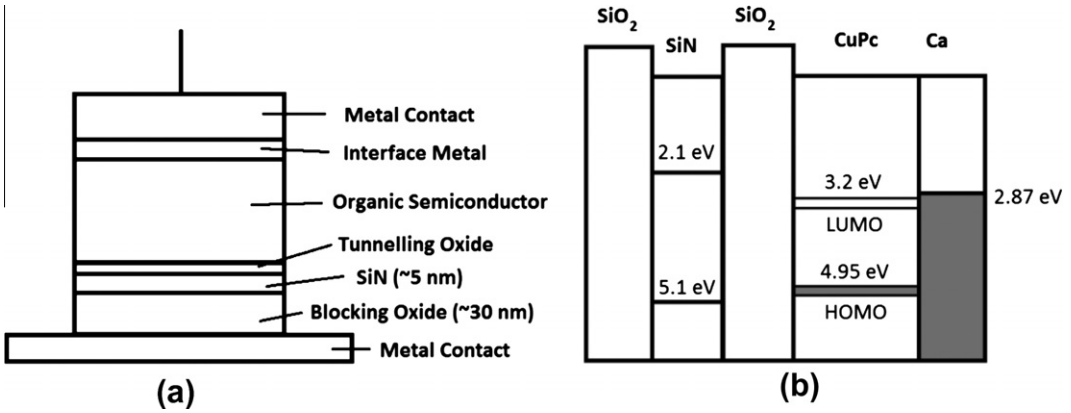

Fig. 1. SONOS structure. (a) Structural cross section. (b) Energy band diagram.

a semiconductor into a silicon nitride charge storage layer when subjected to applied voltages which are higher than the normal operating voltage of the transistor. This charge will act to shift the TFT threshold voltage and provide an intrinsic memory structure. The charge retention period has been shown to vary depending on the SONOS structure [5–9] and can be used to mimic long and short-term memories.

The SONOS gate structure is shown in Fig. 1. Here we show a device with a calcium interface layer for electron injection into the LUMO level of the CuPc. Previous work on the organic SONOS structures has shown that the tunneling proceeds through the thin oxide layer into traps in the forbidden region of the SiN.

3. Experimental

The SONOS layers were deposited using a high vacuum inductively coupled plasma chemical vapour deposition (ICPCVD) system. All devices utilized 2-in n-type silicon wafer substrates to ensure flatness. For the CuPc devices, metal bottom contacts were deposited on top of a thick buffer oxide, followed by the SONOS layer deposition. The SONOS layers were as follows; tunneling oxide (silicon dioxide – SiO_2) of 1 nm, a 5 nm silicon nitride (SiN) charge trapping layer, and 30 nm SiO_2 blocking layer. Control devices with only the blocking oxide were also fabricated. Next the CuPc and top metal contacts were deposited.

A transmission electron microscopy (TEM) image of a calibration SONOS structure (2 nm SiO_2, 5 nm SiN, 1.5 nm SiO_2) on a-Si:H is shown in Fig. 2a confirming the presence of the layers and the verification of the approximate thicknesses. An Energy Dispersive Spectroscopy (EDS) scan of oxygen content is shown in Fig. 2b with a clear dip in O_2 concentration at the depth of the SiN layer. The EDS scan is of a structure of 1.5 nm SiO_2, 5 nm SiN, 2 nm SiO_2. The devices were measured using an HP 4280 CV Meter.

TFTs were prepared in the following manner; Silicon wafers were used to ensure flatness. The wafers were cleaned using ultrasonic baths of acetone and methanol followed by a buffered HF etch. A 100 nm thick thermal oxide was grown on these wafers followed by a 100 nm thick CVD oxide. Next, the gate was deposited using titanium, which was then patterned and etched. Next a 36 nm SONOS oxide structure (30 nm SiO_2, 5 nm SiN, 1 nm SiO_2) was deposited in an ICPCVD. Next, source drain contacts were deposited using titanium, patterned and then etched. Next, a thin calcium layer was thermally deposited, followed by a 100 nm layer of CuPc. The device was then encapsulated using a cover glass and UV curable sealing epoxy. The devices were then measured using an HP 4155 Semiconductor parameter analyzer.

4. Results and discussion

The CV characteristics for the organic (CuPc) capacitor with 1 nm tunneling oxide organic device are shown in

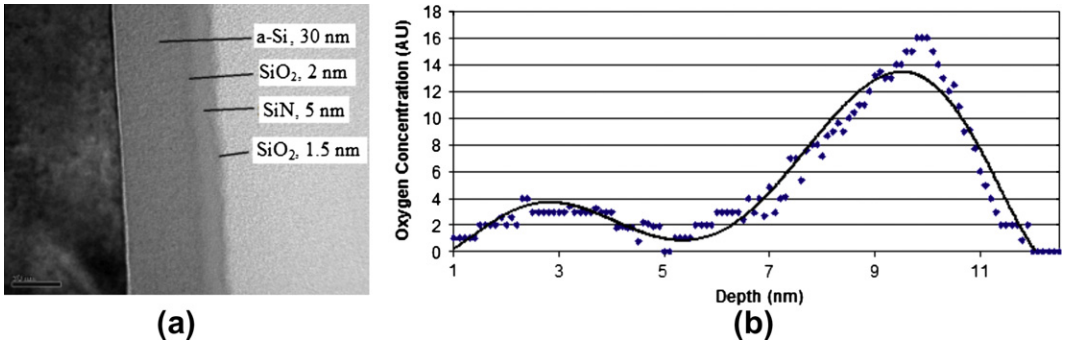

Fig. 2. (a) TEM of SONOS stack showing 2 nm SiO_2, 5 nm SiN, 1.5 nm SiO_2 structure. (b) EDS scan of SONOS stack.

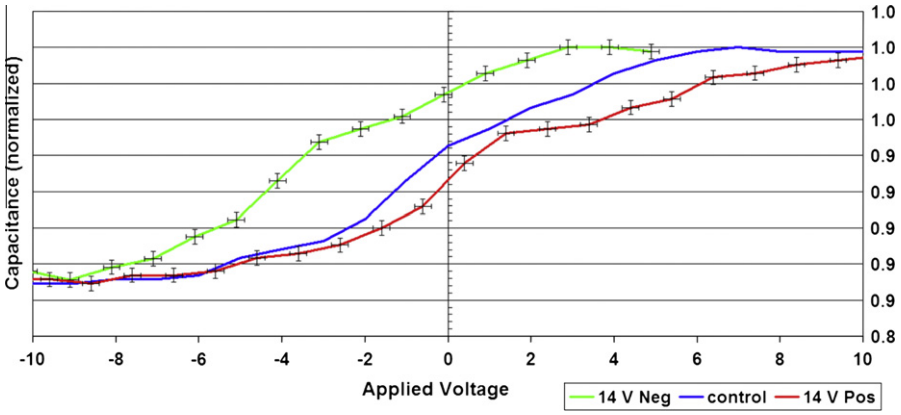

Fig. 3. CuPc organic SONOS device capacitance–voltage scan of control samples and 1 nm tunneling oxide samples after +14 V and −14 V charging.

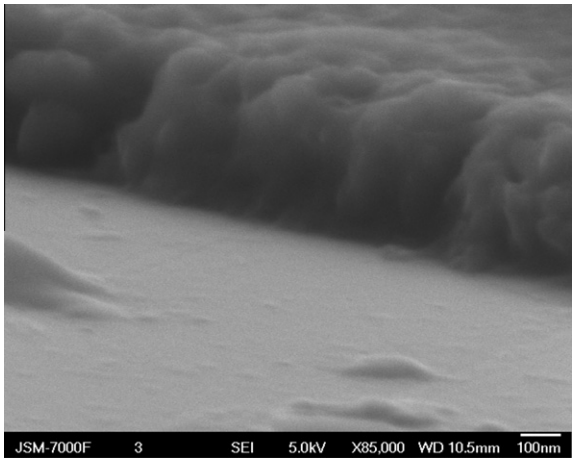

Fig. 4. FESEM of oxide–CuPc interface.

Fig. 3. Here there is a clear shift in the threshold voltage of approximately 4 V with applied bias of ±14 V. Also shown is the control device with the blocking oxide only. No significant shift in the control device behavior was observed for applied charging voltages of ±14 V. The interface layer between the oxide and organic layers is shown in Fig. 4. No crystalline interface state is visible. This is consistent with the behavior of the control device which does not show any significant memory effect.

Representative transfer characteristics for a single gate SONOS CuPc n type device are shown in Fig. 5. This device requires further optimization but it will be seen that it can be used in the modeled performance of the analog circuits. The two curves represent the Ids characteristics of the device at 30 V, with one curve after biasing the gate at +14 V and with the second curve after a bias of −14 V. The average shift in effective applied voltage is seen to be approximately 3 V. (It varies over the applied voltage range.) With this structure, an applied 14 V corresponds to a V_{ox} across the tunneling oxide 540 meV. Based on this V_{ox} range, tunneling is likely into interfacial traps 500 meV below the SiN conduction band rather than directly into the SiN conduction band itself. The maximum entrapped charge in the SiN layer was found to be on the order of 0.1 C/m^2. At an effective V_{ox} of 540 meV, the theoretical maximum tunneling current density is on the order of 150 μA/cm^2, indicating that a 1 μm^2 TFT device has a charging time on the order of 1 ns. These results were used to model the analog neural circuits.

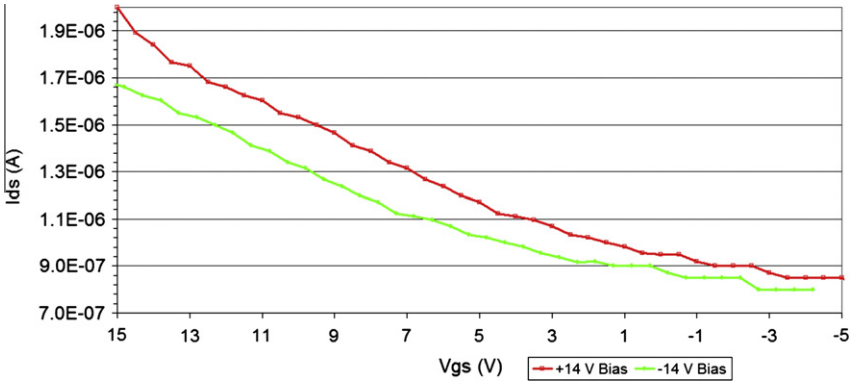

Fig. 5. Transfer characteristics of CuPc SONOS TFT with 1 nm tuneling oxied. Scans after both +14 V and −14 V charging.

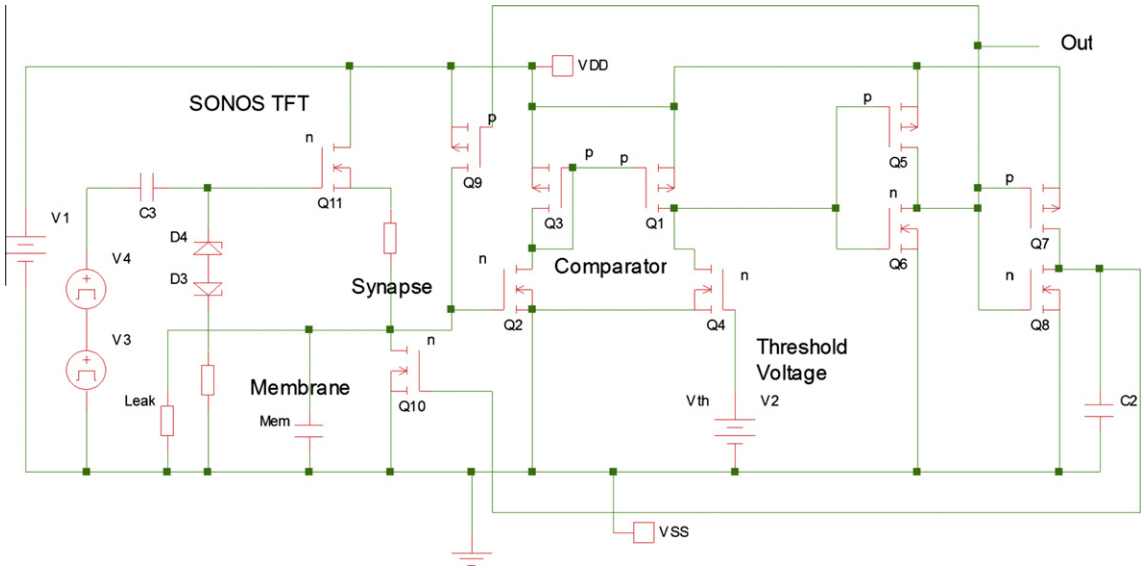

Fig. 6. Spiking analog neural circuit with SONOS OTFT. SONOS TFT is at Q11 and includes capacitor C3 and opposing diodes D3 and D4.

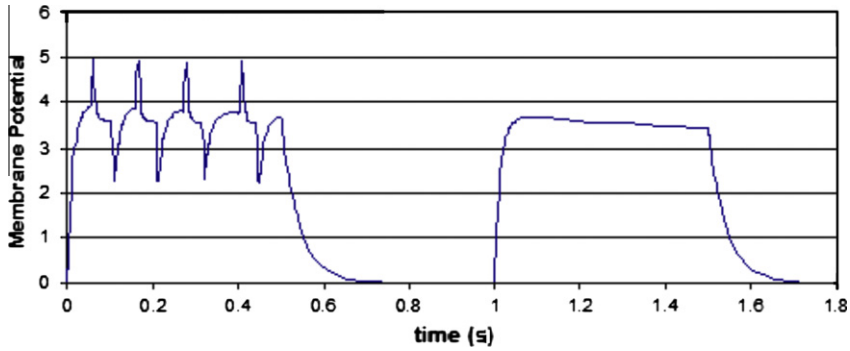

Fig. 7. Output spiking behavior and adaptation of the basic analog spiking neural circuit. Input voltage pulses of 0.5 s were applied to capacitor C3 at $t = 0$ s and $t = 1$ s.

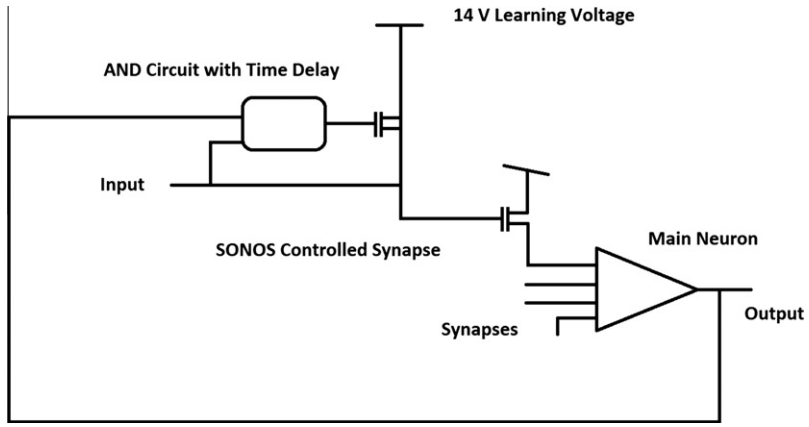

Fig. 8. Hebbian learning circuit. The output of the main neuron is combined (AND) with a time delayed main input to control a 14 V learning pulse.

A spiking circuit described by van Schaik [10] was used as a starting point for the proposed circuit. The original circuit was first modified to work with the single gate standard OTFTs [1–4]. The modified circuit is shown in Fig. 6.

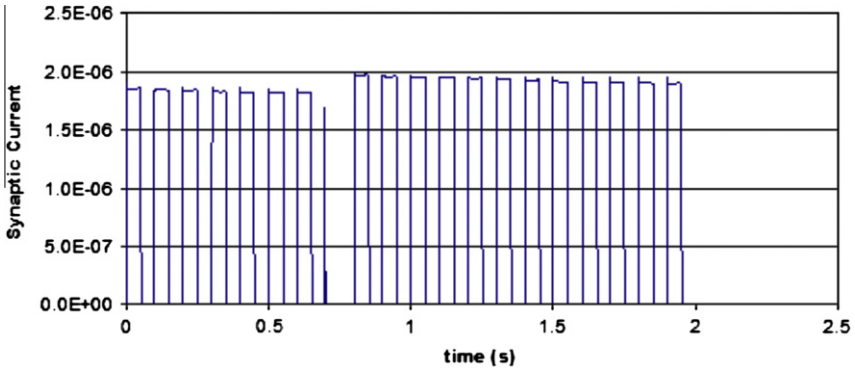

Fig. 9. Synaptic current modification. A learning pulse is applied at $t = 0.75$ s to SONOS TFT at Q11.

In this circuit, the membrane potential (at C Mem) is compared (through circuit Q1, Q2, Q3, Q4) to a threshold voltage (V2) and sets a local output voltage to high or low. A following circuit (Q6 and Q5) inverts this voltage and drives a current (through Q10), that simulates sodium current, that charges the membrane capacitor (C Mem). A second inverter (Q7, Q8) controls the current (through Q9) that discharges the membrane through a potassium like current. The SONOS transistor is shown at Q11, providing a single synapse. In a full device, numerous synapses will exist in parallel. A simulation of the membrane potential from this circuit is shown in Fig. 7. Here we can see the spiking behavior as well as short term adaptation as a second input pulse at 1 s is insufficient to reach the threshold voltage.

A model of the SONOS gate for transistor Q11 is included in Fig. 6 as can be seen by capacitor C3 and opposing zener diodes D3 and D4.

A learning schematic for the SONOS TFT is shown in Fig. 8. The main spiking circuit is represented by the integrator, with only a single synapse connected. The output of this neuron is combined with an AND circuit with the original synaptic input (with time delay circuitry). This circuit behavior was simulated using the voltage pulse sources, V3 and V4 (shown in Fig. 6). The learning ability is shown in Fig. 9, as the synaptic current through Q11 is increased after a learning pulse from V4 at 0.7 s.

5. Conclusions

This work successfully demonstrated the use of amorphous organic transistors with SONOS memory structures with a Hebbian learning circuit in spiking neuron-like circuits. The ability to adjust the TFT characteristics of amorphous transistors combined with the manufacture-ability of the devices makes these transistors aptly suitable for use in the design of complex analog neural networks with high connectivity and unsupervised learning capability. The embedded Hebbian learning circuits and the ability to stack amorphous organic cells in 3-dimensional circuits allows for the design and manufacture of high-density circuits.

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